ABSTRACT OF THE DISCLOSURE

The present invention provides a delay analysis system which makes it possible to make delay analysis considering circuit logical information in order to give more accurate delay times. In addition to circuit connection information and delay time information on the rises and falls of the input and output terminals of the circuits which are stored in a delay analysis library, the delay analysis system according to the present invention contains, in the library, logical operation information which represents correspondence between the logical values of each input terminal and their output logical values of the circuits . When making the delay analysis of a logic circuit, the system selects, for each circuit included in the logic circuit, a delay time between an input terminal and an output terminal from the delay time information on the rises and falls of the input and output terminals of the basic circuits, stored in the library, according to the logical operation of the circuit in order to calculate the delay time of the circuit.